DRONACHARYA
GROUP OF INSTITUTIONS

INTEGRATED CIRCUITS LAB

LABORATORY MANUAL

B.TECH. Semester -V

Subject Code: KEC-551

Session: 2023-24, Odd Semester

DRONACHARYA GROUP OF INSTITUTIONS
DEPARTMENT OF ECE
#27 KNOWLEDGE PARK 3
GREATER NOIDA

AFFILIATED TO Dr. A P J ABDUL KALAM TECHNICAL UNIVERSITY

LUCKNOW

List of Experiments mapped with COs

S. No.	Name of the Experiments	COs
1.	Inverting Amplifier	CO1
2.	Non - Inverting Amplifier	CO1
3.	Differentiator	CO2
4.	Integrator	CO2
5.	Second Order Active Low Pass Filter	CO2
6.	Square Wave Generator	CO3
7.	Schmitt Trigger	CO3
8.	Design of Instrumentation Amplifier	CO5
9.	RC Phase Shift Oscillator	CO5
10.	Wein Bridge Oscillator	CO4
11.	Monostable Multivibrator	CO4
12.	Astable Multivibrator	CO4
13.	PLL Characteristics	CO5
14.	Frequency Multiplier Using PLL	CO5
15.	IC Voltage Regulator: (Using Ic 723)	CO5

INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

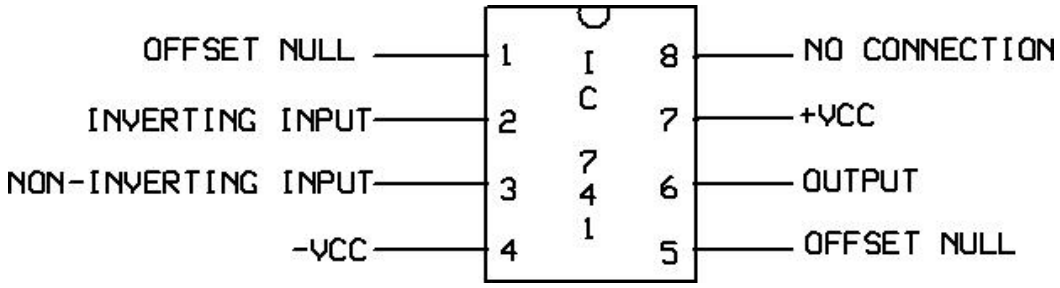
$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

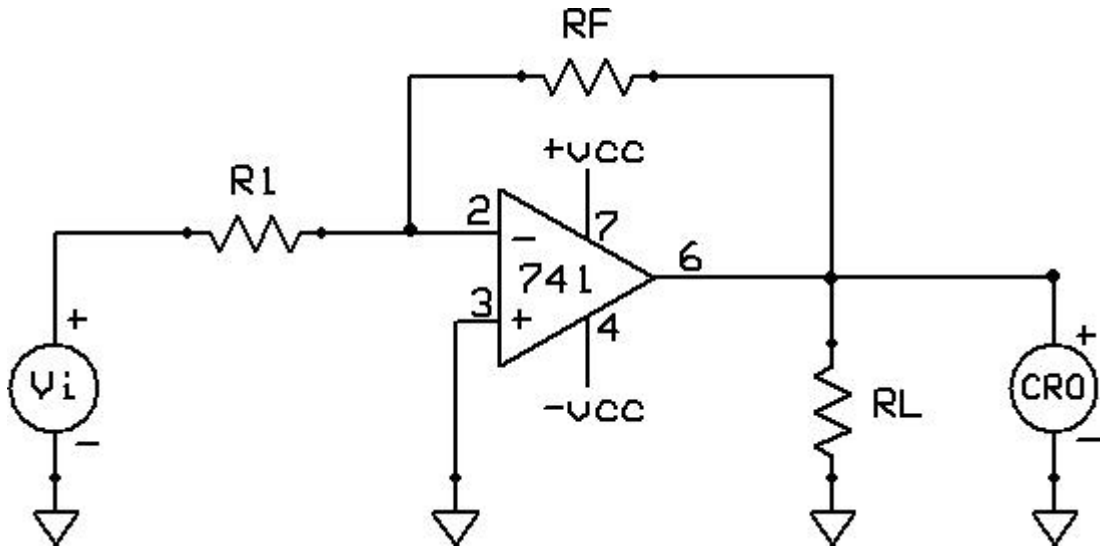
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



DESIGN:

We know for an inverting Amplifier $A_{CL} = R_F / R_1$

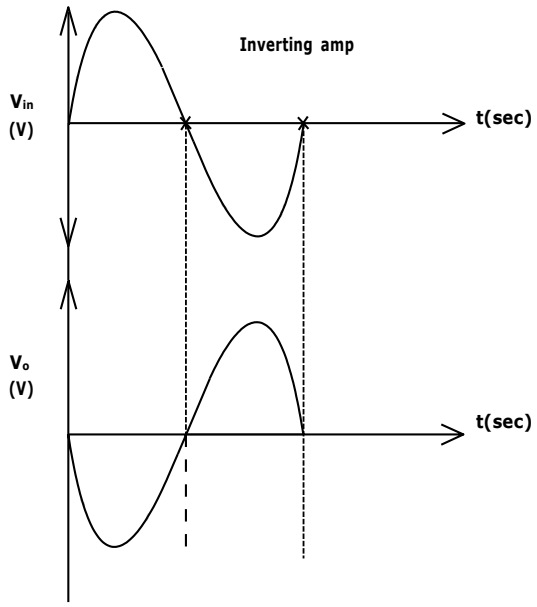
Assume R_1 (approx. 10 KΩ) and find R_f

Hence $V_o = - A_{CL} V_i$

OBSERVATIONS:

S.No		Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

MODEL GRAPH:



RESULT:

2. NON - INVERTING AMPLIFIER

AIM:

To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$V_o = A_{CL}\ V_i$$

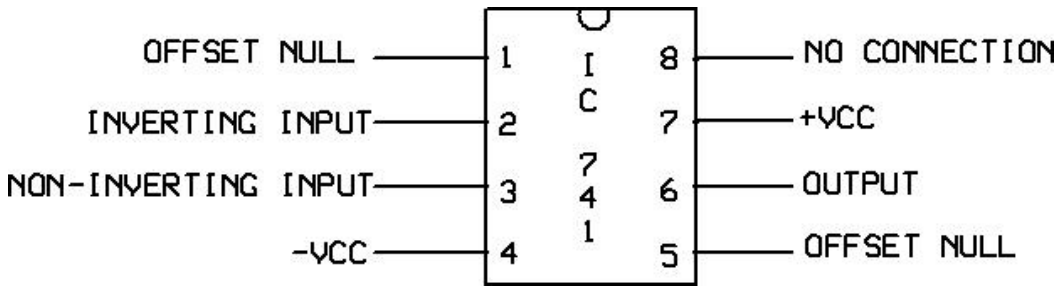
Here the output voltage is in phase with the input signal.

PROCEDURE:

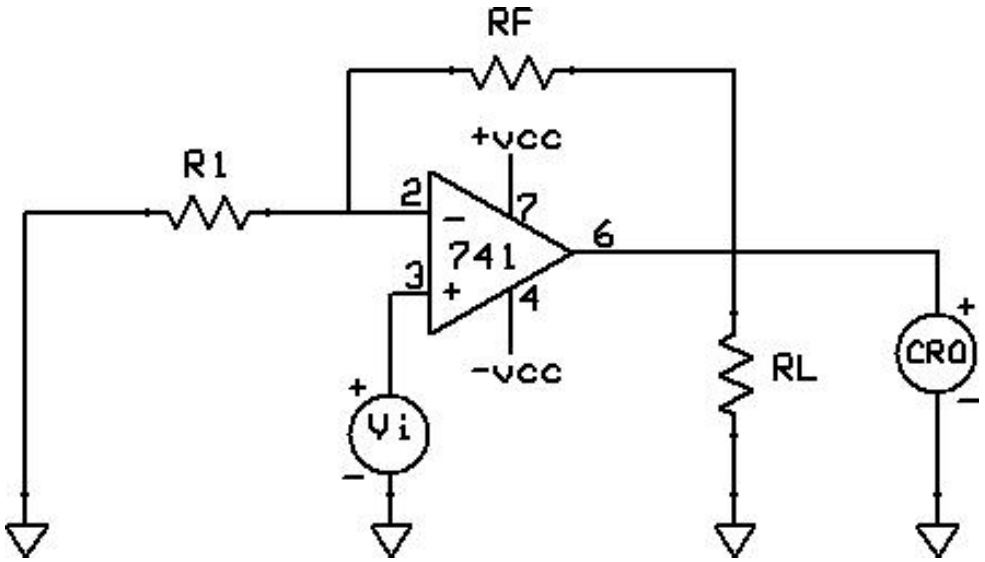
1. Connections are given as per the circuit diagram.
2. $+V_{cc}$ and $-V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.

4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



DESIGN:

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$

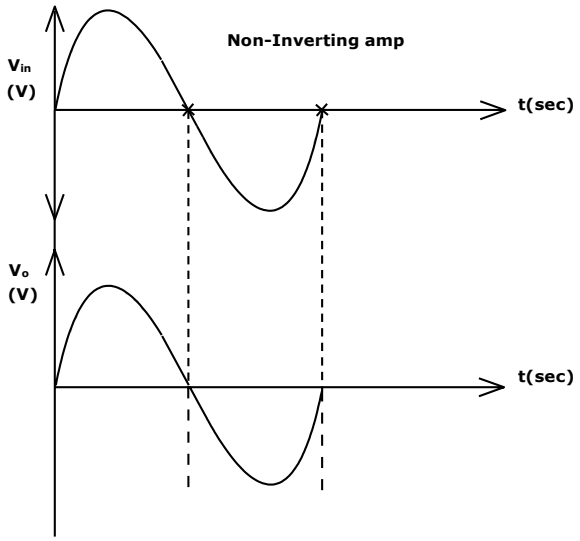
Assume R_1 (approx. 10 KΩ) and find R_f

Hence $V_o = A_{CL}\ V_i$

OBSERVATIONS:

S.No		Input	Output	
			Practical	Theoretical
1.	Amplitude (No. of div x Volts per div)			
2.	Time period (No. of div x Time per div)			

MODEL GRAPH:



RESULT:

3. DIFFERENTIATOR

AIM:

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. The expression for the output voltage is given as,

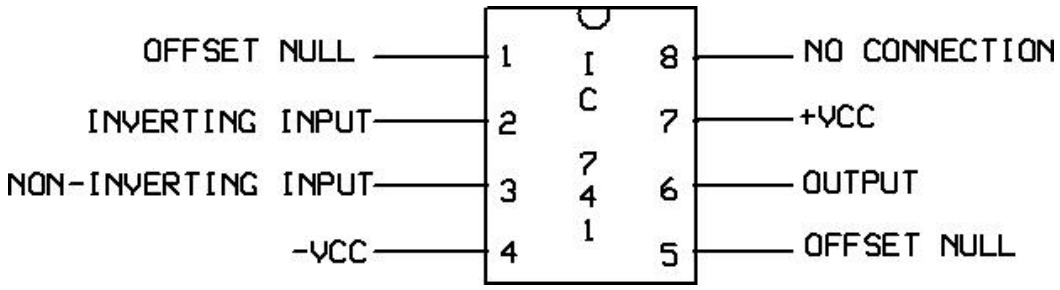
$$V_o = - R_f C_1 (dV_i / dt)$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

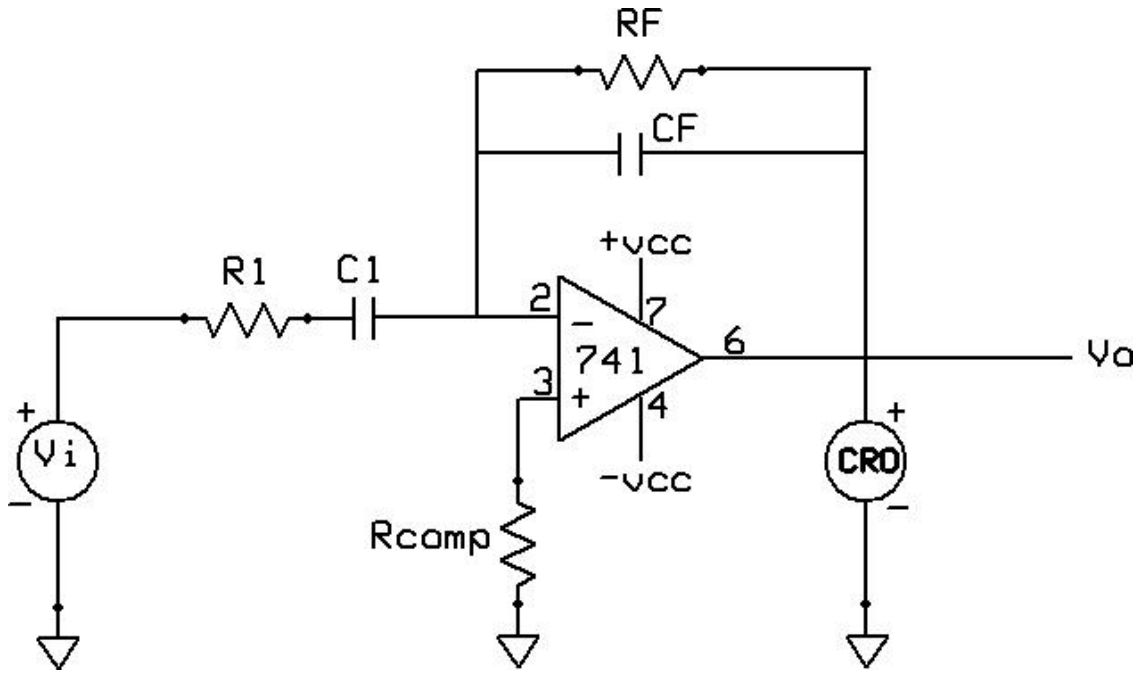
1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ μF, calculate the value of R_f.
2. Choose $f_b = 20\ f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$.

The differentiator is most commonly used in waveshaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF DIFFERENTIATOR:



DESIGN :

[To design a differentiator circuit to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1 V peak at 1000Hz is applied to the differentiator , draw its output waveform.]

Given $f_a = 1$ KHz

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$

Let us assume $C_1 = 0.1$ μF ; then

$R_f =$ _____

Since $f_b = 20 f_a$, $f_b = 20$ KHz

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$

Hence $R_1 =$ _____

Also since $R_1C_1 = R_f C_f$; Cf = _____

Given $V_p = 1$ V and f = 1000 Hz, the input voltage is $V_i = V_p \sin \omega t$

We know $\omega = 2\pi f$

Hence $V_o = - R_f C_1 (dV_i/dt)$

$= - 0.94 \cos \omega t$

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

RESULT:

4. INTEGRATOR

AIM:

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as,

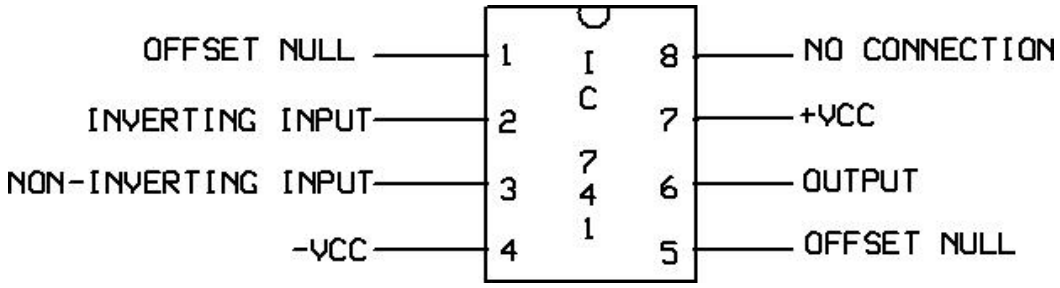
$$V_o = - (1/R_f C_1) \int V_i \, dt$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is,

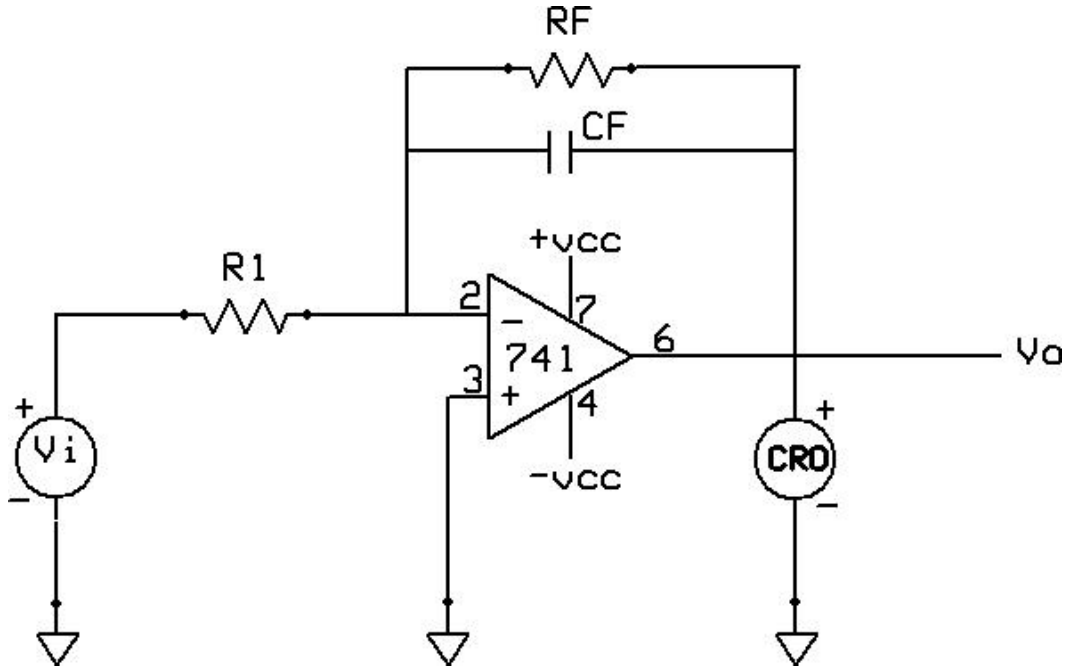
$$T \geq R_f C_f$$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



DESIGN:

[To obtain the output of an Integrator circuit with component values R_1C_f = 0.1ms , R_f = 10 R_1 and C_f = 0.01 μF and also if 1 V peak square wave at 1000Hz is applied as input.]

We know the frequency at which the gain is 0 dB, $f_b = 1 / (2\pi R_1 C_f)$

Therefore f_b = _____

Since $f_b = 10 f_a$, and also the gain limiting frequency $f_a = 1 / (2\pi R_f C_f)$

We get , R_1 =_____and hence R_f = _____

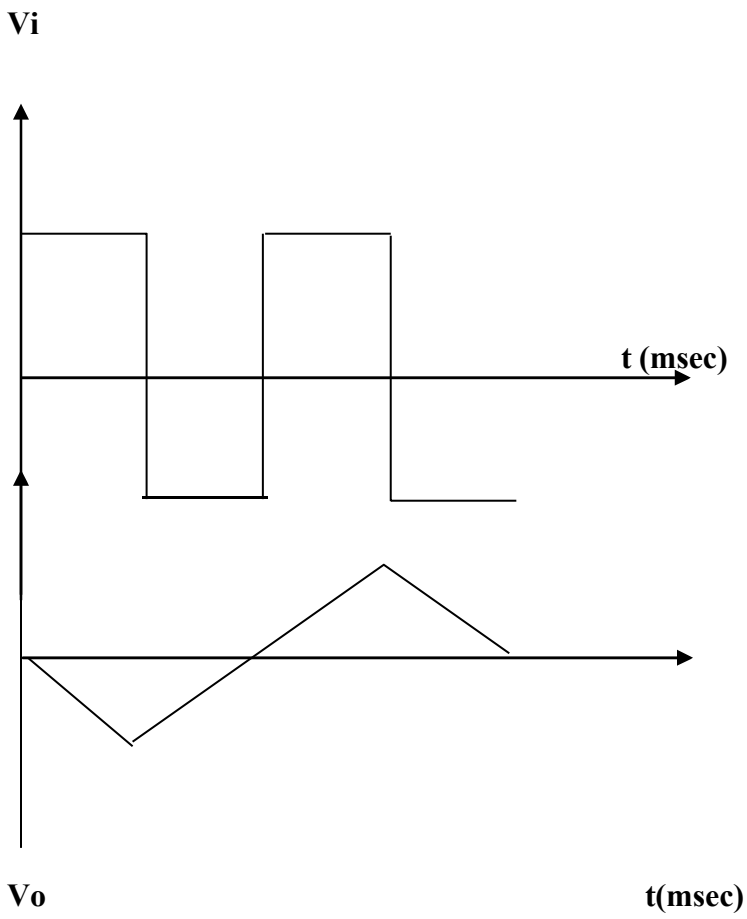
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

MODEL GRAPH: INTEGRATOR



RESULT:-

5. SECOND ORDER ACTIVE LOW PASS FILTER

AIM:

Design a second order active Butterworth low pass filter having upper cut off frequency 1 KHz, also determine its frequency response using IC 741.

APPARATUS REQUIRED :

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC741	1
2	RESISTOR	10KΩ, 1.5KΩ 5.6 KΩ	1 1 1
3	Capacitor	0.1 μF	1
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

DESIGN:

Given: f_H = 1 KHz = 1/ (2πRC)

Let C = 0.1 μF, R = 1.6 KΩ

For n = 2, α (damping factor) = 1.414,

Passband gain = A_o = 3 - α =3 – 1.414 = 1.586.

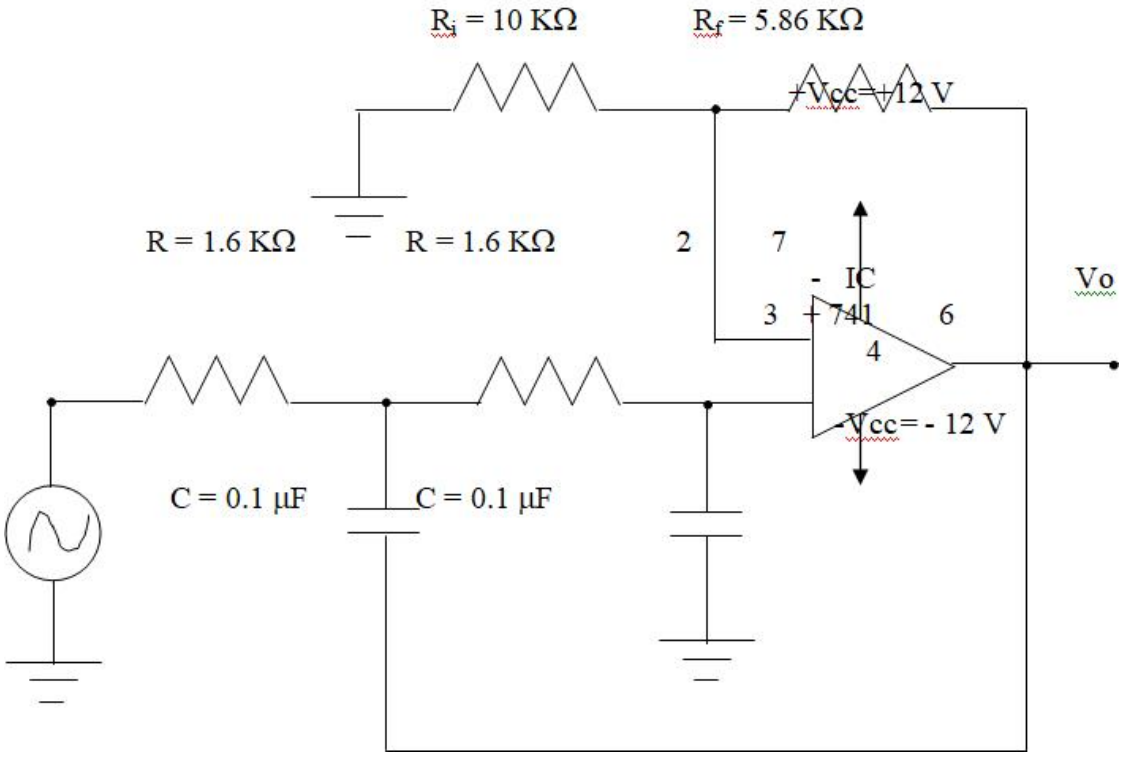
Transfer function of second order butterworth LPF as:

$$H(s) = \frac{1.586}{S^2 + 1.414\,s + 1}$$

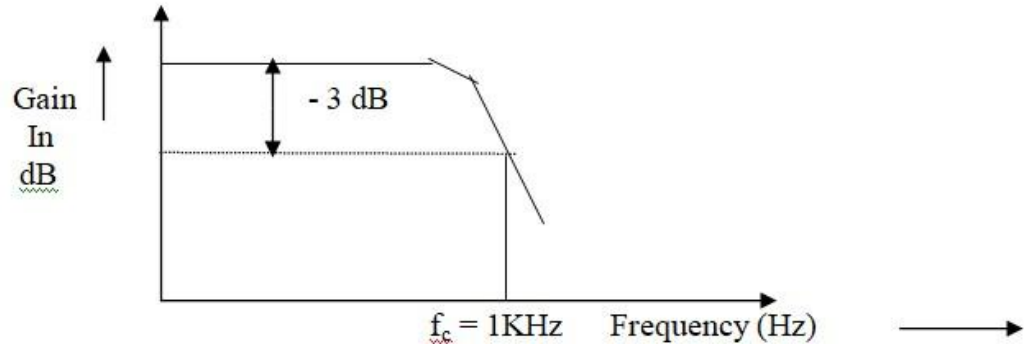
Now $A_o = 1 + (R_f / R_1) = 1.586 = 1 + 0.586$

Let R_i = 10 KΩ, then R_f = 5.86 KΩ

CIRCUIT DIAGRAM:



Frequency Response Characteristics: (Use Semi – log Graph):



THEORY:

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two RC pairs and has a roll-off rate of -40 dB/decade. A general second order filter (Sallen Kay filter) is used to analyze different LP, HP, BP and BSF.

PROCEDURE :

The connections are made as shown in the circuit diagram. The signal which has to be made sine is applied to the RC filter pair circuit with the non-inverting terminal. The supply voltage is switched ON and the o/p voltages are recorded through CRO by varying different frequencies from 10 Hz to 100 KHz and tabulate the readings. Calculating Gain through the formula and plotting the frequency response characteristics using Semi-log graph sheet and finding out the 3 dB line for f_c.

OBSERVATION:

V_{IN} = 1 Volt

S.No.	FREQUNCY Hz	O/P voltage V_O Volts	Av=20 log Vo/Vi dB

RESULT:

6. SQUARE WAVE GENERATOR

AIM:

To design a square wave generator circuit for the frequency of Oscillations of 1KHZ

APPARATUS REQUIRED :

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC741	1
2	RESISTOR	4.7KΩ, 1KΩ 1.16KΩ	1 1 1
3	CAPACITOR	0.1μF	1
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

DESIGN:

F=1KHZ =T=1ms

R2=1KΩ,C=0.1μF

R1=1.16R2=1.16KΩ≅1KΩ+100Ω

T=2RC

R=T/2C =5KΩ

≅4.7KΩ

THEORY:

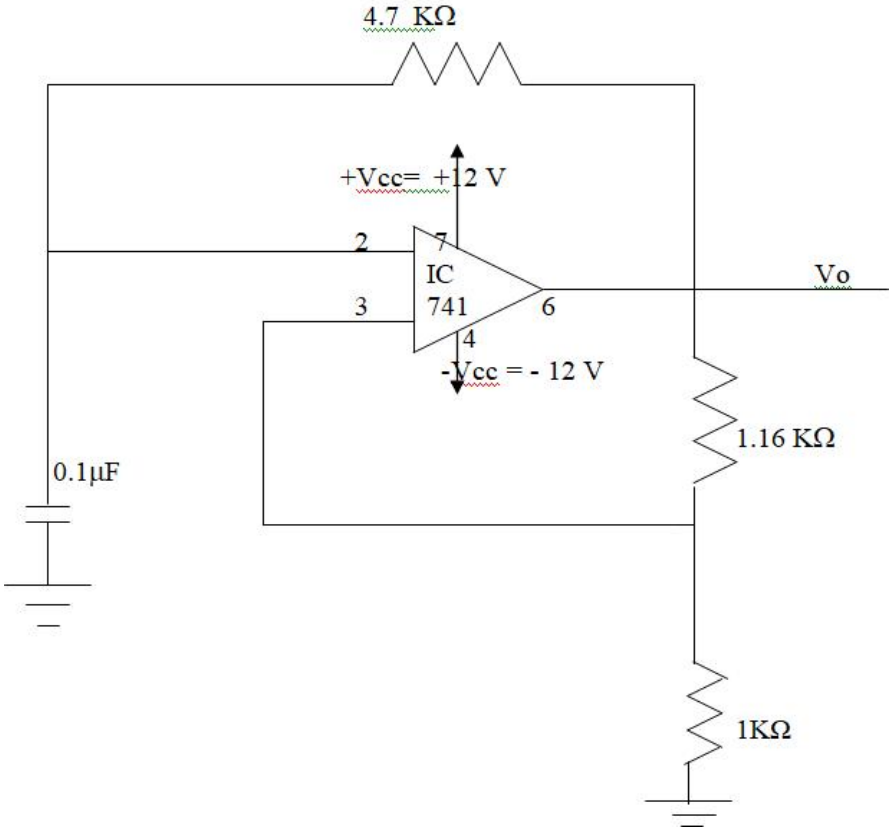
A simple op-Amp square wave generator is also called as free running oscillator, the principle of generation of square wave output is

to force an op-amp to operate in the saturation region . A fraction β=R2/(R1+R2) of the output is fed back to the (+) input terminal. The output

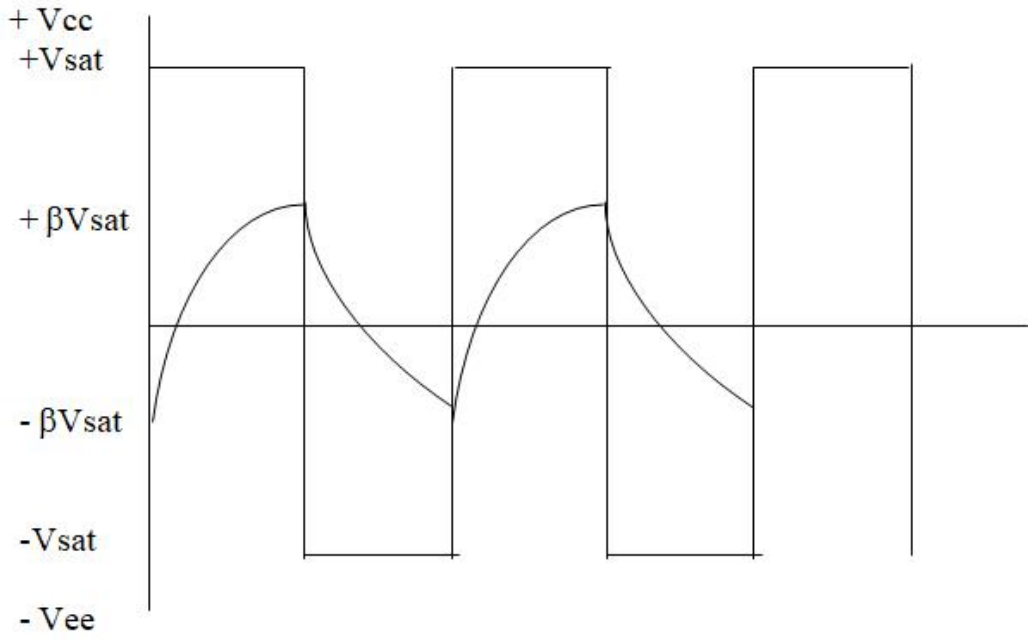
is also fed to the (-) terminal after integrating by means of a low pass Rc combination in astable multivibrator both the states are quasistables.

the frequency is determined by the time taken by the capacitor to charge from- βVsat to+βVsat.

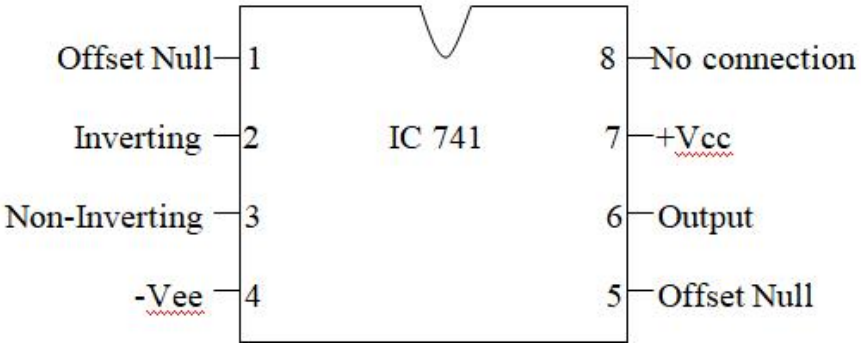
CIRCUIT DIAGRAM:



MODEL GRAPH:



Pin Diagram:



RESULT:

7. SCHMITT TRIGGER

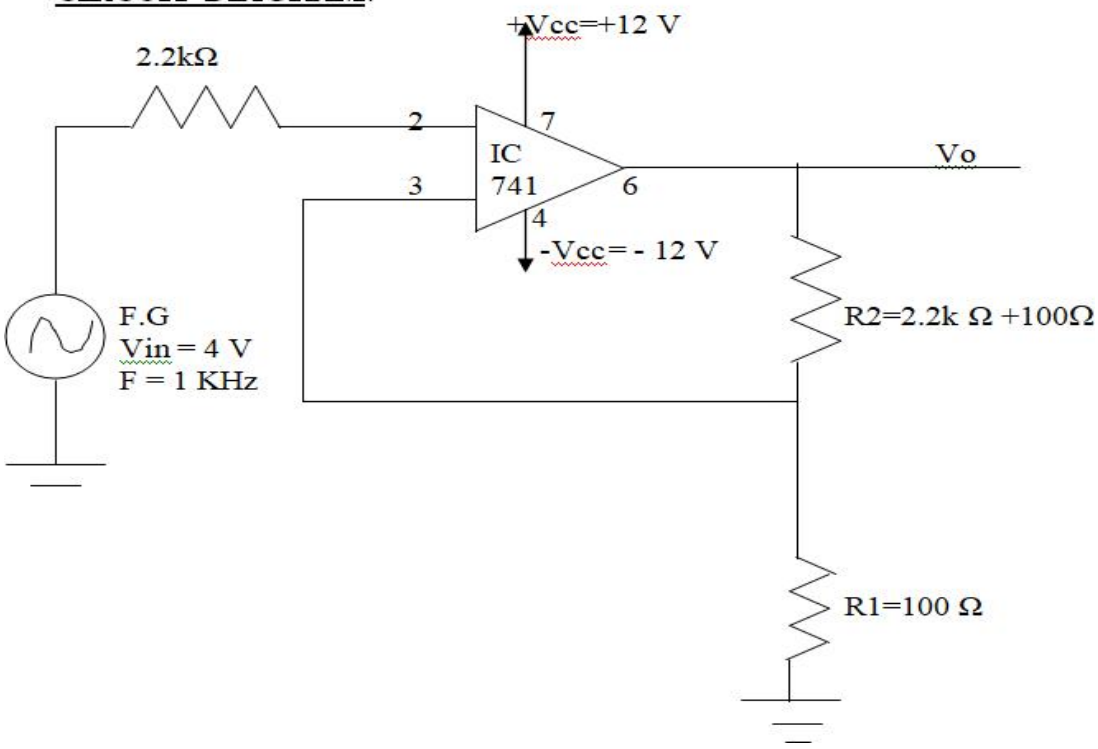
AIM:

To study the Schmitt trigger using IC 741.

APPARATUS REQUIRED :

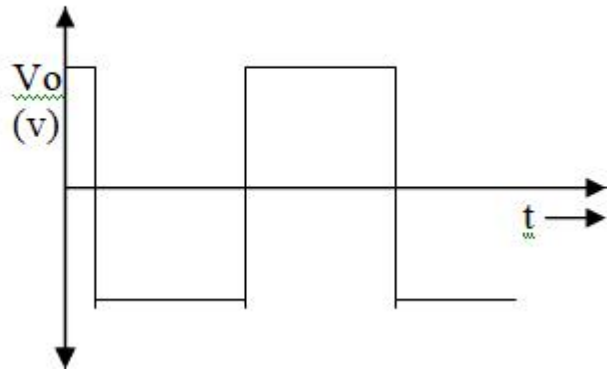
S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC741	1
2	RESISTOR	100KΩ, 2.2KΩ	2, 1
3	CRO	-	1
4	RPS	DUAL(0-30) V	1

CIRCUIT DIAGRAM:



Pin Diagram:

O/P wave form:



THEORY:

Schmitt trigger is useful in squaring of slowly varying i/p waveforms.Vin is applied to inverting terminal of op-amp .Feedback voltage is applied to the non-inverting terminal. LTP is the point at which output changes from high level to low level .This is highly useful in triangular waveform generation, wave shape pulse generator, A/D convertor etc.

PROCEDURE :

- The connections are made as shown in the circuit diagram.
- The signal which has to be made square is applied to the inverting terminal .

- Here the i/p is a sine waveform.The supply voltage is switched ON and the o/p waveform is recorded through CRO.
- The UTP and LTP are also found and the theoretical and practical values are verified.

$$LTP = R1/ (R1 + R2) ^{X(-Vsat)}$$

$$UTP = R2 /(R1 + R2) ^{X(+Vsat)}$$

Design :

+Vsat= +Vcc=15v

-Vsat= -Vee= -15v

RESULT:

8. DESIGN OF INSTRUMENTATION AMPLIFIER

Aim:

Design of Instrumentation Amplifier with Digital Indication and to study its working.

Apparatus required:

Instrumentation Amplifier Kit

Digital multimeter

Connecting wires

Procedure:

1. Patch the connections and connect the design resistance Rg extending to have the desired gain.

2. Measure the input voltage at Vin1 and Vin2 using digital multimeter.

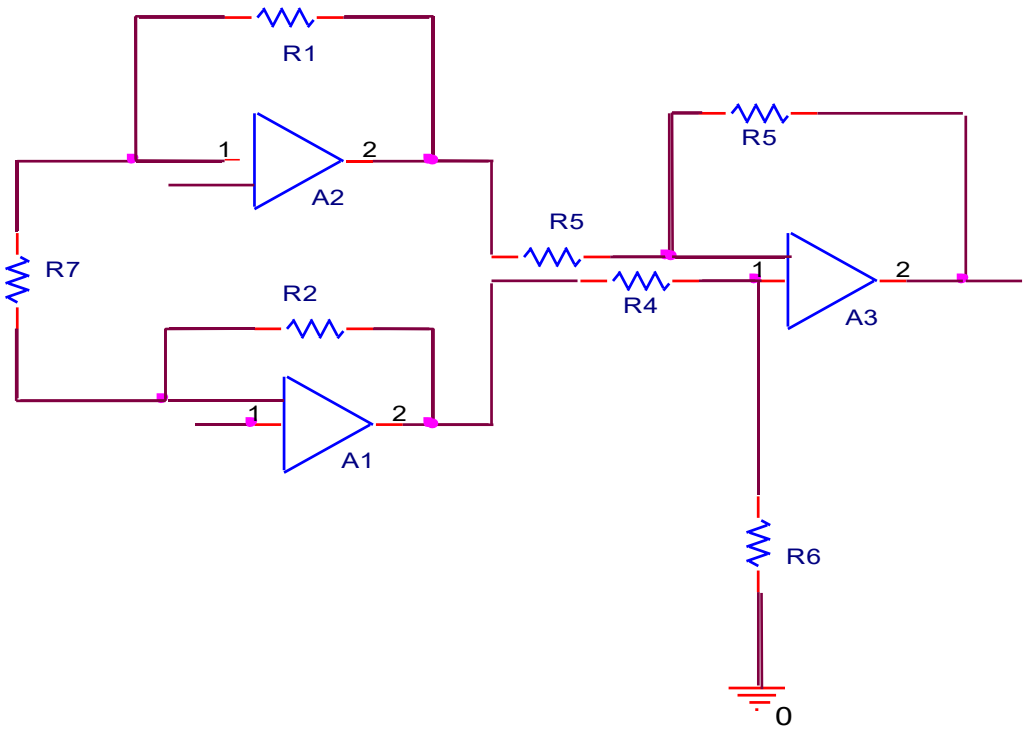
3. The difference in Vin2- Vin1 is amplified and indicated in LCD display.

4. Check the theoretical value with the experimental value.

TABULATION:

S.No	THEORETICAL VALUE					PRACTICAL VALUE
	GAIN SETTING	V_{IN1} (mv)	V_{IN2} (mv)	$V_{IN2} - V_{IN1}$	Vout (mv)	GAIN = Vout/ $V_{IN2} - V_{IN1}$

CIRCUIT DIAGRAM:



Result:

9. RC PHASE SHIFT OSCILLATOR

AIM:

To construct a RC phase shift oscillator to generate sine wave using op-amp.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC-741	1
2	RESISTOR	16KΩ, 32KΩ, 1.59KΩ,	1 2
3	CAPACITOR	0.1μf	2
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

THEORY:

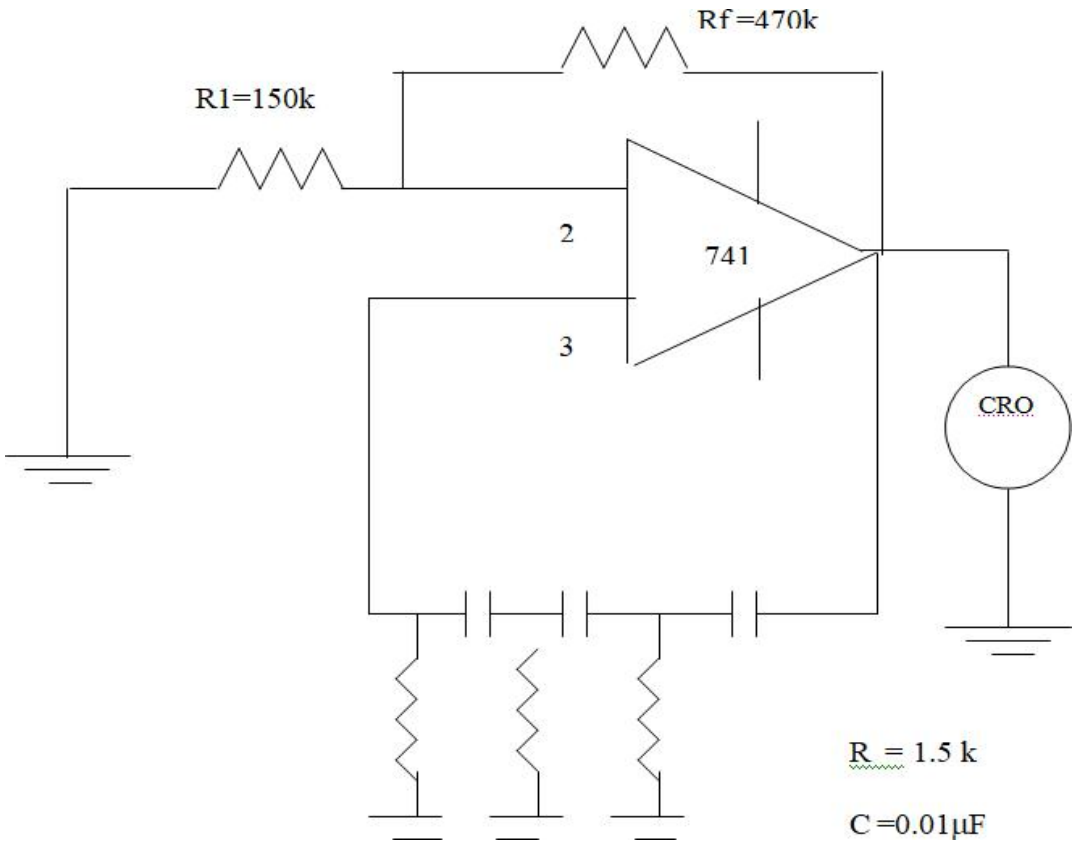
Basically, positive feedback of a fraction of output voltage of a amplifier fed to the input in the same phase, generate sine wave.

The op-amp provides a phase shift of 180 degree as it is used in the inverting mode. An additional phase shift of 180 degree is provided by the feedback Rc network.The frequency of the oscillator f_o is given by

$$f_o = 1 / \sqrt{6}\,(2\,\pi\,R\,C)$$

Also the gain of the inverting op-amp should be at least 29, or $R_f \geq 29\ R_1$

RC PHASE SHIFT OSCILLATOR



Design:

$f_o = 1 / \sqrt{6}(2\pi R C)$

$R_f \geq 29 R_1$

C = 0.01μF, fo = 500 Hz.

$R = 1 / \sqrt{6}(2\pi f C) = 13$ k

Therefore, Choose R = 15k

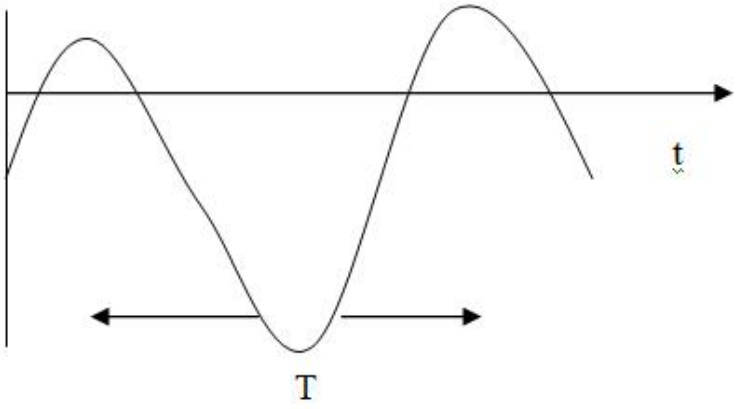
To prevent loading,

$R1 \geq 10 R$

R1 =10 R = 150 k.

$R_f = 4.35$ M

MODEL GRAPH:



Observations:

Time period =

Frequency =

Amplitude =

Procedure:

1. Connect the circuit as shown in fig. With the design values.
2. Observe the output waveforms using a CRO.For obtaining sine wave adjust Rf.
3. Measure the output wave frequency and amplitude.

Result:

10. WEIN BRIDGE OSCILLATOR

AIM:

To construct a wein bridge oscillator for fo = I khz and study its operation.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC-741	1
2	RESISTOR	16KΩ, 32KΩ,1.59KΩ,	1, 2
3	CAPACITOR	0.1μf	2
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

THEORY:

In wein bridge oscillator ,wein bridge circuit is connected between the amplifier input terminals and output terminals . The bridge has a series rc network in one arm and parallel network in the adjoining arm. In the remaining 2 arms of the bridge resistors R1and Rf are connected . To maintain oscillations total phase shift around the circuit must be zero and loop gain unity. First condition occurs only when the bridge is p balanced . Assuming that the resistors and capacitors are equal in value ,the resonant frequency of balanced bridge is given by

$$Fo = 0.159 / RC$$

Design :

At the frequency the gain required for sustained oscillations is given by

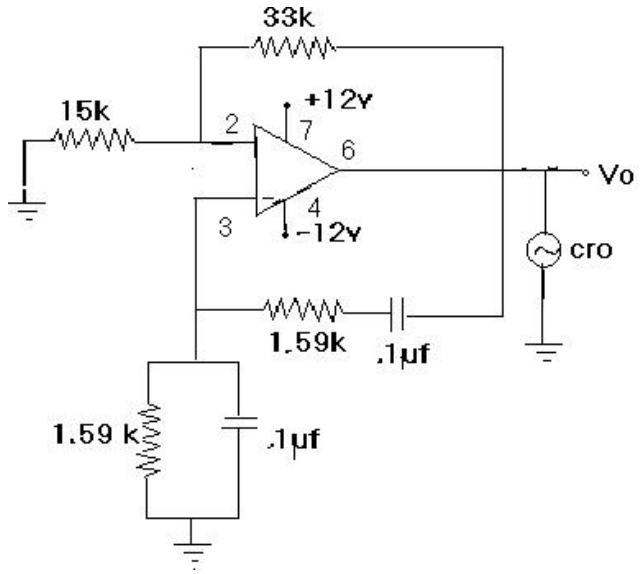
$1+Rf/R1 = 3$ or $Rf = 2R1$

$Fo = 0.65/RC$ and $Rf = 2R1$

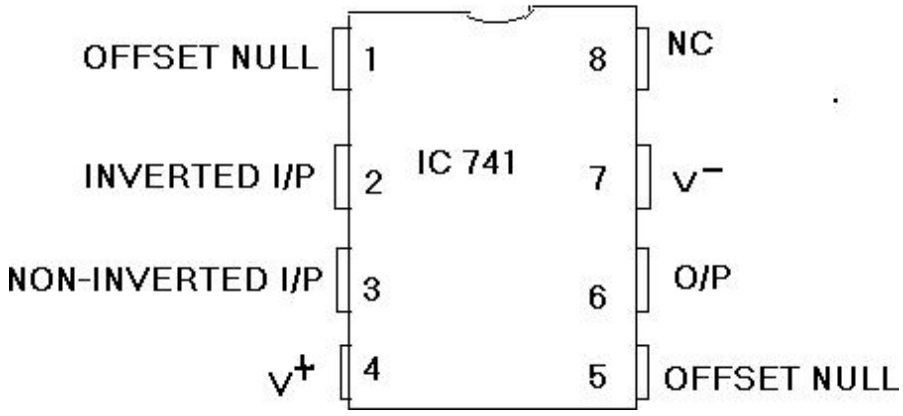
Calculation: Theoretical

Fr = 1/(2*3.14*R*C)

CIRCUITDIAGRAM



PIN DIAGRAM:



Calculation:

Theoretical: F = 1/(2*3.14*R*C)

Practical: F = 1/T

PROCEDURE:

- Connections are made as per the diagram .
- R,C,R1,Rf are calculated for the given value of Fo using the design
- Output waveform is traced in the CRO .

RESULT :

11. MONOSTABLE MULTI VIBRATOR

AIM:

Design the monostable multivibrator using the IC555.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	9KΩ	1
3	CAPACITOR	0.01μF, 0.1μF	1, 1
4	RPS	(0-30) V	1
5	CRO	-	1

THEORY:

A monostable multivibrator has one stable state and a quasistable state. When it is triggered by an external agency it switches from the stable state to quasistable state and returns back to stable state. The time during which it states in quasistable state is determined from the time constant RC. When it is triggered by a continuous pulse it generates a square wave. Monostable multi vibrator can be realized by a pair of regeneratively coupled active devices, resistance devices and op-amps.

DESIGN :

$T = 0.1ms$

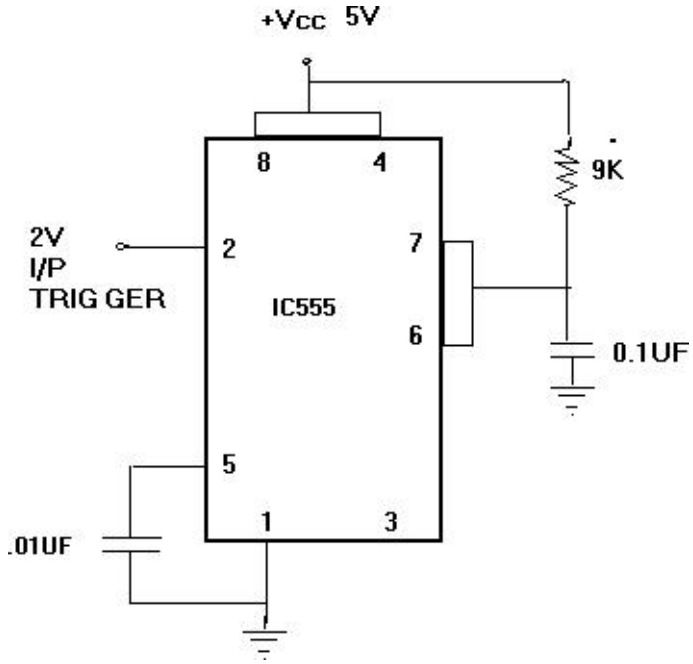
$C = 0.01\mu F$, **$T = 1.096RC$**

$R = T / 1.096C = (0.1*10^{-3}) / (1.096*0.01*10^{-6})$

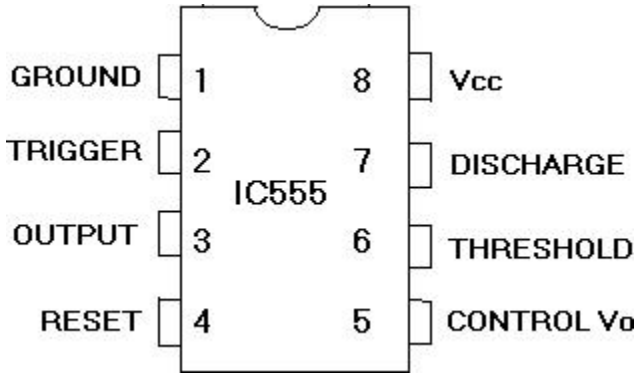
$= 9.12\ K\Omega$

$R \cong 9\ K\Omega$

CIRCUIT DIAGRAM :



PINDIAGRAM:



PROCEDURE:

- The connections are made as per the diagram.
- The value of R is chosen as 9kΩ.
- The DCB is set to the designed value.
- The power supply is switched on and set to +5V.
- The output of the pulse generator is set to the desired frequency.
- Here the frequency of triggering should be greater than width of ON period (i.e.) T >W.

- The output is observed using CRO and the result is compared with the theoretical value.
- The experiment can be repeated for different values of C and the results are tabulated.

OBSERVATION

C (uf)	Theoritical(T=1.095 RC(ms)))	Practical T(ms)

RESULT:

12. ASTABLE MULTIVIBRATOR

Aim:

To study the application of IC555 as an astable multivibrator.

APPARATUS REQUIRED :

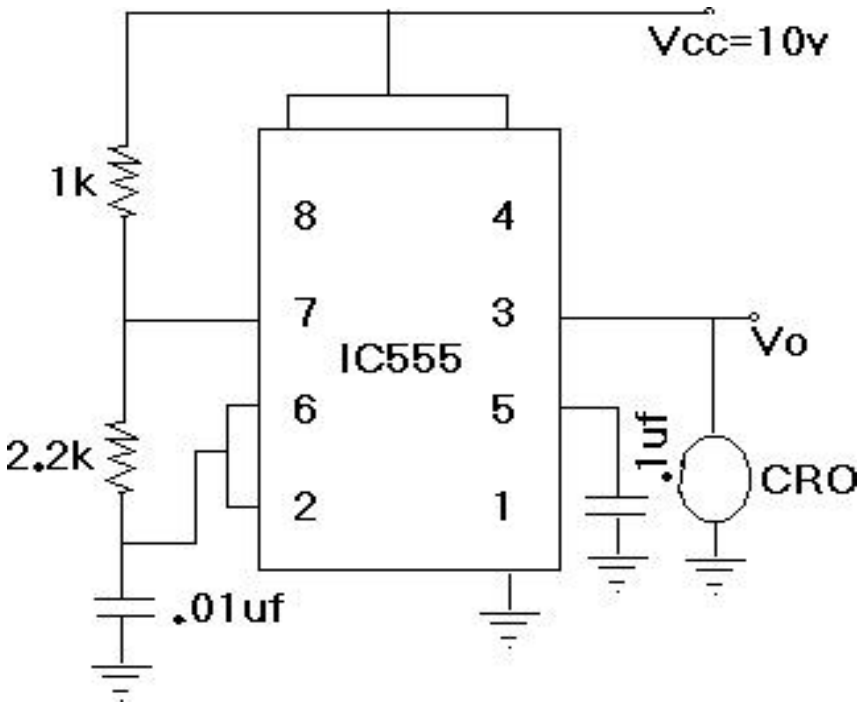
S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	1KΩ, 2.2KΩ	1, 1
3	CAPACITOR	0.1μF, 0.01μF	1, 1
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

Theory:

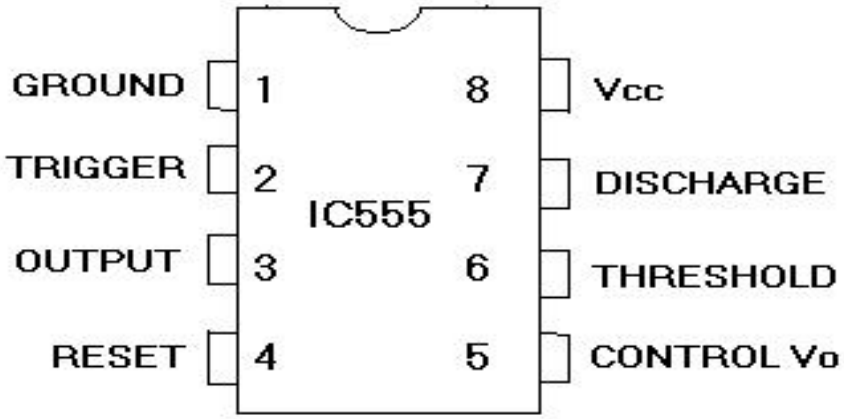
The IC555 timer is a 8 pin IC that can be connected to external components for astable operation. The simplified block diagram is drawn. The OP-AMP has threshold and control inputs. Whenever the threshold voltage exceeds the control voltage, the high output from the OP –AMP will set the flip-flop. The collector of discharge transistor goes to pin 7. When this pin is connected to an external trimming capacitor, a high Q output from the flip flop will saturate the transistor and discharge the capacitor. When Q is low the transistor opens and the capacitor charges.

The complementary signal out of the flip-flop goes to pin 3 and output. When external reset pin is grounded it inhibits the device. The on – off feature is useful in many application. The lower OP- AMP inverting terminal input is called the trigger because of the voltage divider. The non-inverting input has a voltage of +Vcc/3, the OP-Amp output goes high and resets the flip flop.

Circuit diagram:



PIN DIAGRAM:



Procedure :

- The connections are made as per the circuit diagram and the values of R and C are calculated assuming anyone term and they are settled .
- The output waveform is noted down and graph is drawn and also the theoretical and practical time period is verified.

Observation:

C (uf)	Theoretical time period(us)	Practical time period(us)	Theoretical freq (kHz)	Practical freq(kHz)

Calculation:

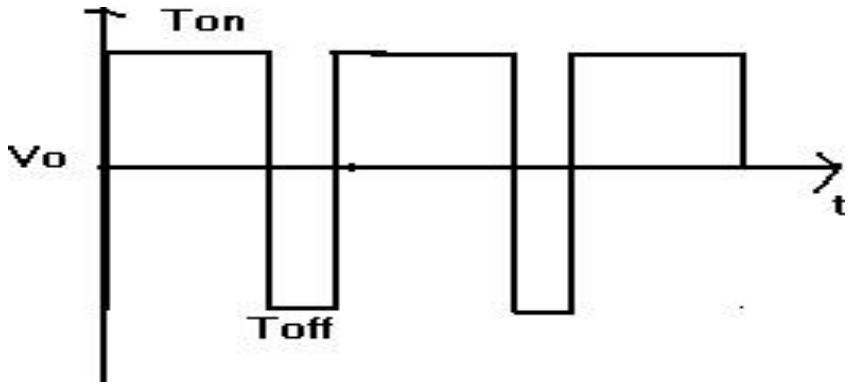
Theoretical:

$T = 0.69(Ra+Rb)C=0.69(1*10^3 + 2.2*10^3)*0.01*10^{-6}) = 0.22\mu s$

Practical:

T = Ton + Toff

MODEL GRAPH:



Result :

13. PLL CHARACTERISTICS

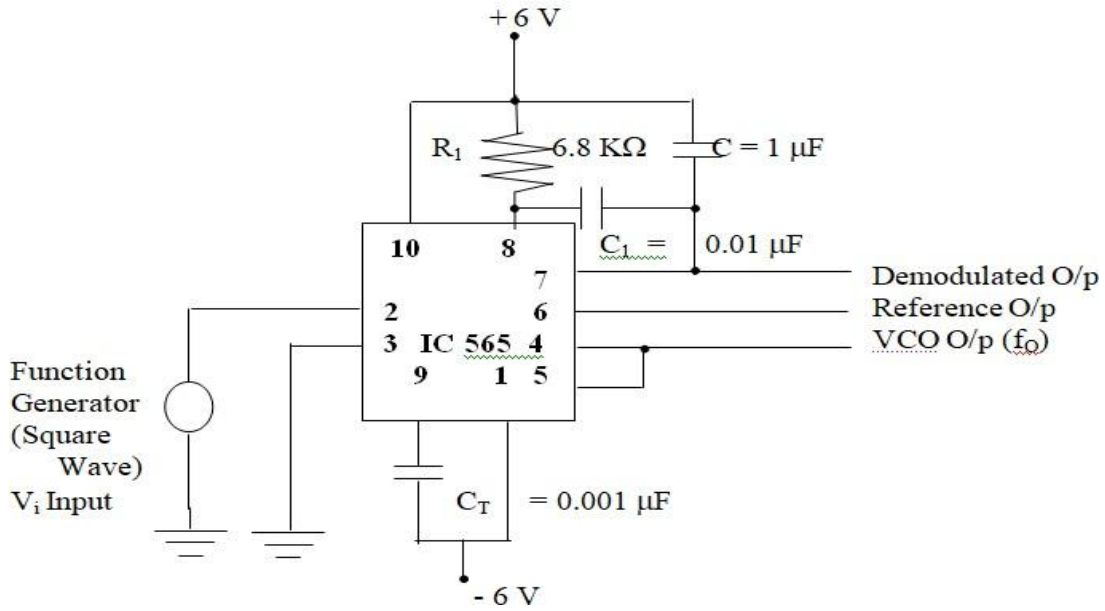
Aim:

To construct and study the operation of PLL IC 565 and determine its Characteristics.

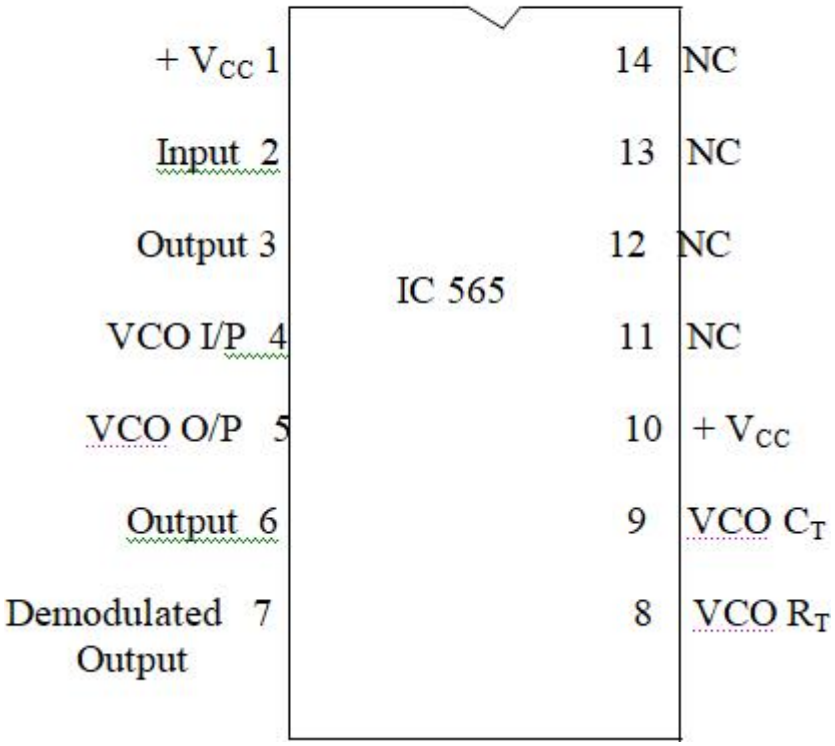
Apparatus Required:

S.No	Components	Range	Quantity
1	IC 565	-	1
2	Resistors	6.8 KΩ	1
3	Capacitors	0.001 μF 0.1 μF, 1 μF	1 each
4	FunctionGenerator (Digital)	1 Hz – 2 MHz	1
5	C.R.O	-	1
6	Dual Power Supply	0- 30 V	1

Circuit Diagram:



Pin Diagram (IC 565 - PLL)



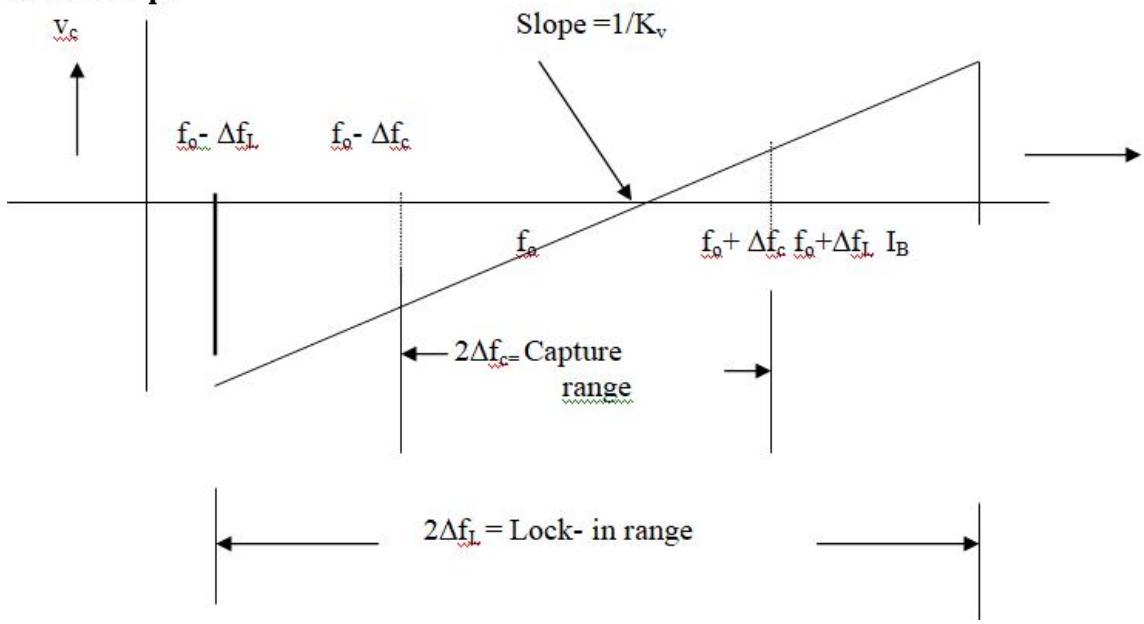
Procedure:

1. The connections are given as per the circuit diagram.
2. Measure the free running frequency of VCO at pin 4, with the input signal V_i set equal to zero. Compare it with the calculated value = $0.25 / (R_T C_T)$.
3. Now apply the input signal of 1 V_{PP} square wave at a 1 KHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.
4. Gradually increase the input frequency till the PLL is locked to the input frequency.This frequency f1 gives the lower end of the capture range.Go on increasing the input frequency, till Pll tracks the input signal,say ,to a frequency f2.This frequency f2 gives the upper end of the lock range.If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the Pll is again locked.This is the frequency f3,the upper end of the capture range.Keep on decreasing the input frequency until the loop is unlocked.This frequency f4 gives the lower end of the lock range.

6. The lock range Δf_L = (f2 – f4).Compare it with the calculated value of ± 7.8 fo / 12. Also the capture range is Δf_c = (f3 – f1).Compare it with the calculated value of capture range.

$$\Delta f_c = \pm (\Delta f_L / (2\pi)(3.6)(10^3) C)^{1/2}$$

Model Graph



Result :

14. FREQUENCY MULTIPLIER USING PLL

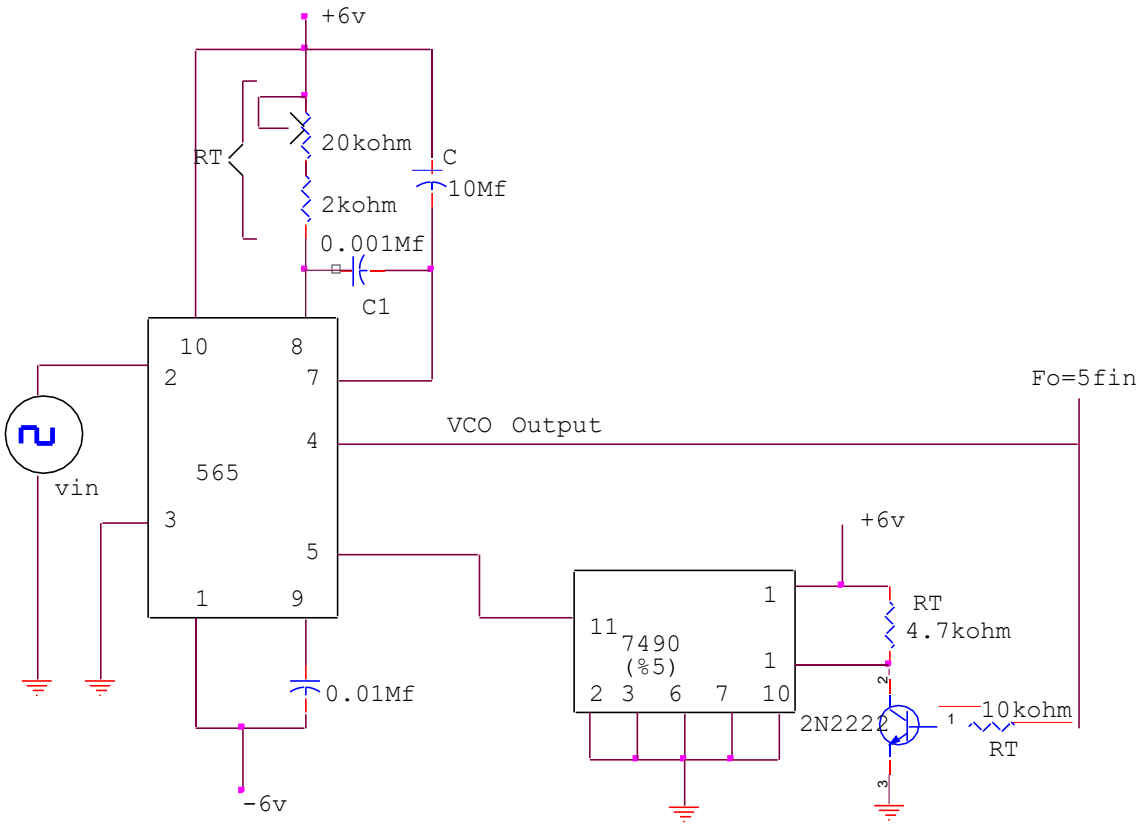
Aim:

To construct and study the operation of frequency multiplier using IC 565.

Apparatus Required:

S.No	Components	Range	Quantity
1	IC 565,IC 7490,2N2222	-	1
2	Resistors	20 KΩ, 2kΩ, 4.7kΩ,10kΩ	1
3	Capacitors	0.001 μF 10 μF	1 each
4	FunctionGenerator (Digital)	1 Hz – 2 MHz	1
5	C.R.O	-	1
6	Dual Power Supply	0- 30 V	1
7.			

Circuit Diagram:



Procedure:

1. The connections are given as per the circuit diagram.
2. The circuit uses a 4- bit binary counter 7490 used as a divide-by-5 circuit.
3. Measure the free running frequency of VCO at pin 4, with the input signal V_i set equal to zero. Compare it with the calculated value = $0.25 / (R_T C_T)$.
4. Now apply the input signal of 1 V_{PP} square wave at 500 Hz to pin 2.
5. Vary the VCO frequency by adjusting the 20kΩ potentiometer till the PLL is locked.Measure the output frequency.It should be 5 times the input frequency.
6. Repeat steps 4,5 for input frequency of 1 kHz and 1.5 kHz.

Result :

15. IC VOLTAGE REGULATOR: (Using IC 723)

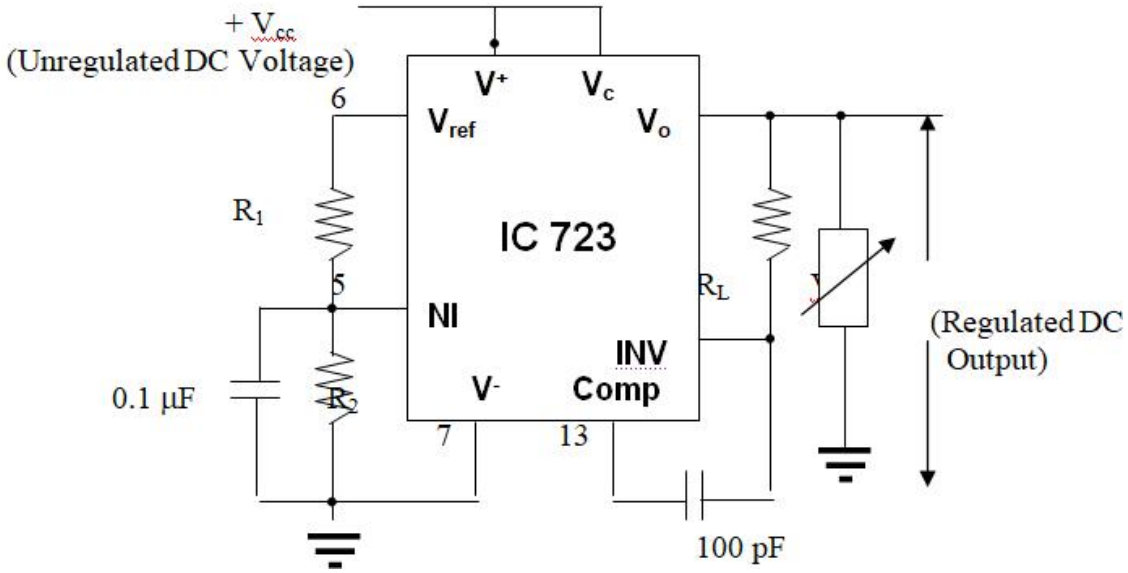
Aim:

Design & Construct a low voltage IC regulator (Using IC 723)

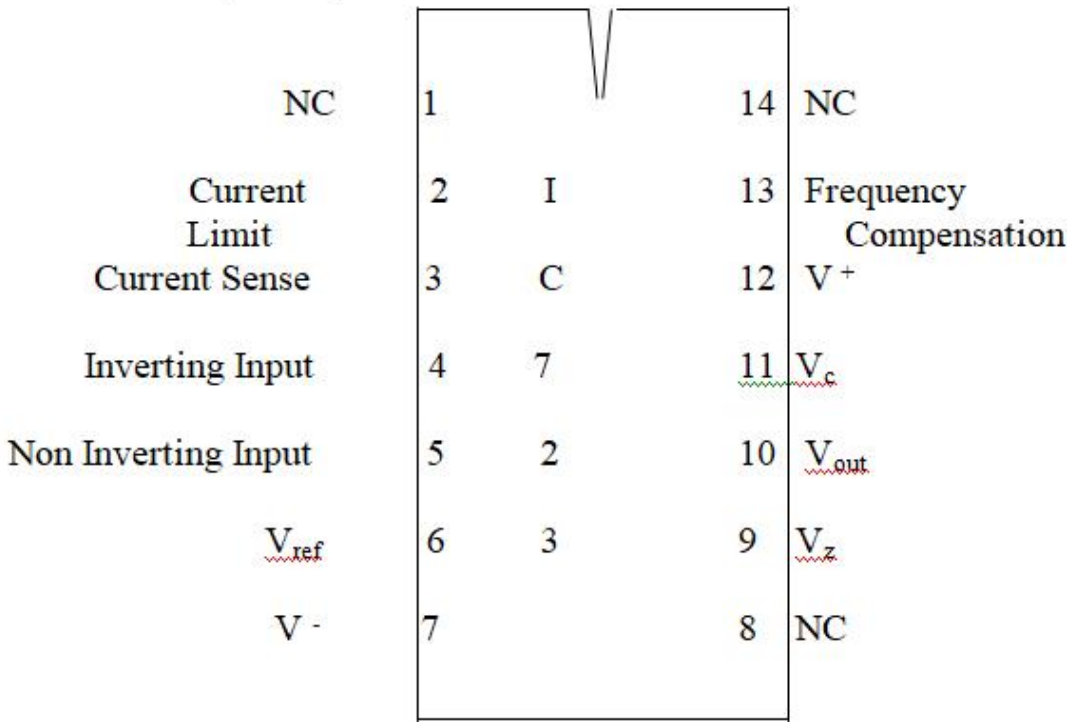
Apparatus Required:

S.No.	ITEM	SPECIFICATION	QTY
1	IC 723		2
2	Resistors		1
3	Capacitors	100 μF / 25 V	2
3	R. P. S	(0- 30) V, 1 mA	1
4	Rheostat	(0-350 Ω), 1.5 A	1
5	Bread Board and Connecting Wires		

Circuit Diagram:



PIN DIAGRAM: (IC 723):



TABULAR COLUMN:

LOAD REGULATION:
INPUT VOLTAGE = Volts

S.No.	LOAD RESISTANCE (Ω)	OUTPUT VOLTAGE (V)

LINE REGULATION:
LOAD RESISTOR = KOhms

S.No.	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)

RESULT:

This lab manual has been updated by

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Please spare some time to provide your valuable feedback.